TRANSLATION

I, Masayuki Horiuchi, residing at 3-36-14, Isobe, Mihama-ku, Chiba-shi, Chiba-ken , Japan, state:

that I know well both the Japanese and English languages,

that I translated, from Japanese into English, Japanese Patent Application No. 2002-274807, filed on September 20, 2002, and

that the attached English translation is a true and accurate translation to the best of my knowledge and belief.

Dated: August 16, 2004

Masayuki Horiuchi

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[Title of the Invention] SEMICONDUCTOR PACKAGE AND METHOD OF FABRICATING THE SAME

[What is claimed is]

[Claim 1] A semiconductor package characterized by comprising a semiconductor substrate including a device region on one surface side thereof and a connecting pad electrically connected to the device region, a support substrate formed on the one surface of the semiconductor substrate, an external electrode formed on other surface side of the semiconductor substrate, and a connecting means, partially extended outside the semiconductor substrate and electrically connecting the connecting pad and external electrode.

[Claim 2] In the invention according to claim 1, the semiconductor package characterized in that the connecting means includes a distribution wire extended to the other surface side of the semiconductor substrate.

[Claim 3] In the invention according to claim 1, the semiconductor package, characterized in that the connecting means includes a connecting wire having one end portion connected to the connecting pad, and the other end portion extended outside the semiconductor substrate.

[Claim 4] In the invention according to claim 3, the semiconductor package, characterized in that the connecting wire includes a metal layer formed of plating.

[Claim 5] In the invention according to claim 3, the semiconductor package, characterized in that the connecting wire includes a portion in close contact with one surface of the semiconductor substrate.

[Claim 6] In the invention according to claim 3, the semiconductor package, characterized in that the connecting wire is formed in close contact with the support substrate.

[Claim 7] In the invention according to claim 3, the semiconductor package, characterized by comprising a projecting connecting electrode between the connecting pad and connecting wire.

[Claim 8] In the invention according to claim 3, the semiconductor package, characterized in that an insulating film is formed between the other surface of the semiconductor substrate, which includes the connecting wire extended outside the semiconductor substrate, and the distribution wire.

[Claim 9] In the invention according to claim 2, the semiconductor package, characterized in that the connecting means includes a connecting wire formed on the surface of the support substrate, which opposes the semiconductor substrate, and having one end portion connected to the connecting pad, and the other end portion extended outside the semiconductor substrate, and a columnar electrode formed on the other end portion of the connecting wire, and the distribution wire is connected to the columnar electrode.

[Claim 10] In the invention according to claim 9, the semiconductor package, characterized in that an insulating film is formed between the other surface of the semiconductor substrate, which includes the connecting wire extended outside the semiconductor substrate and the columnar electrode, and the distribution wire.

[Claim 11] In the invention according to claim 2, the

semiconductor package, characterized in that the external electrode is formed on a connecting pad portion of the distribution wire, and an insulating film is so formed as to cover the other surface of the semiconductor substrate, which includes the distribution wire except for the external electrode.

[Claim 12] In the invention according to claim 11, the semiconductor package, characterized in that the external electrode has a columnar electrode, and a solder ball is formed on the columnar external electrode.

[Claim 13] In the invention according to claim 1, the semiconductor package, characterized in that the device region is a photoelectric conversion device region.

[Claim 14] In the invention according to claim 1, the semiconductor package, characterized in that the support substrate is a glass substrate.

[Claim 15] In the invention according to claim 14, the semiconductor package, characterized in that a transparent adhesive layer or transparent encapsulating layer is provided between the semiconductor substrate and glass substrate.

[Claim 16] A method of fabricating a semiconductor package characterized by comprising the steps of:

forming a plurality of connecting wires on one surface of a wafer-like semiconductor substrate including, on one surface, a plurality of device regions and a plurality of connecting pads each connected to one of said plurality of device regions, such that one end portion of each of said plurality of connecting wires is connected to the corresponding one of the

connecting pads, and the other end portion of the connecting wire is extended outside the corresponding connecting pad;

placing a support substrate on the surface of the semiconductor substrate, which includes said plurality of connecting wires;

exposing the other end portions of said plurality of connecting wires by removing, between the device regions, at least portions of the semiconductor substrate, which correspond to the other end portions of said plurality of connecting wires;

forming an external electrode electrically connected to the other end portion of each connecting electrode; and

obtaining a plurality of semiconductor packages each including the semiconductor substrate with the external electrode, by cutting the support substrate between the device regions.

[Claim 17] In the invention according to claim 16, the method of fabricating a semiconductor package, characterized by comprising a step of thinning the semiconductor substrate by polishing the other surface of the semiconductor substrate, before at least portions of the semiconductor substrate, which correspond to the other end portions of said plurality of connecting wires are removed between the device regions.

[Claim 18] A method of fabricating a semiconductor package, characterizsed by comprising the steps of:

forming connecting wires each extending to a periphery of the inside of each of a plurality of semiconductor mounting regions from an inside of the semiconductor mounting region on

one surface of a supporting substrate having a size corresponding to each of a plurality of semiconductor packages, and forming a columnar electrode on the connecting wire formed on the periphery of each of the semiconductor mounting region;

placing, on the semiconductor mounting region of the support substrate, a semiconductor substrate including a device region on a surface opposite to the support substrate and a connecting electrode around the device region, and connecting the connecting electrode of each semiconductor substrate to the connecting wire formed on the periphery of the inside of the semiconductor mounting region of the corresponding support substrate;

forming an external electrode electrically connected to each columnar electrode; and

obtaining a plurality of semiconductor packages, each having the semiconductor substrate provided with the external electrode, by cutting the supporting substrate between the semiconductor substrates.

[Claim 19] In the invention according to claim 18, the method of fabricating a semiconductor package, characterized in that after the semiconductor substrate is placed on the semiconductor supporting region of the support substrate, an insulating film is so formed as to cover the other surface of the semiconductor substrate, which includes the columnar electrode, and polishing the surface of the insulating film and the other surface of the semiconductor substrate, thereby thinning the semiconductor substrate and exposing an upper surface of the columnar electrode.

[Claim 20] In the invention according to any one of claims 16 to 18, the method of fabricating a semiconductor package, characterized in that the external electrode is formed on a distribution wire formed to be extended to a side of the other surface of the semiconductor substrate.

[Claim 21] In the invention according to claim 20, the method of fabricating a semiconductor package, characterized by comprising a step of forming the external electrode on a connecting pad portion of the distribution wire, and a step of forming an insulating film so as to cover the other surface of the semiconductor substrate, which includes the distribution wire except for the external electrode.

[Claim 22] In the invention according to claim 21, the method of fabricating a semiconductor package, characterized by comprising a step of forming a solder ball on the external electrode.

[Claim 23] In the invention according to any one of claims 16 to 18, the method of fabricating a semiconductor package, characterized in that the device region is a photoelectric conversion device region.

[Claim 24] In the invention according to any one of claims 16 to 18, the method of fabricating a semiconductor package, characterized in that the support substrate is a glass substrate.

[Claim 25] In the invention according to claim 24, the method of fabricating a semiconductor package, characterized by comprising a step of forming a transparent adhesive layer or transparent encapsulating film between the semiconductor

substrate and glass substrate.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

This invention relates to a semiconductor package and a method of fabricating the same.

[0002]

[Prior Art]

A conventional semiconductor package, especially a semiconductor substrate on the major surface of which a photosensitive element such as a CCD (Charge Coupled Device) or transistor is formed is fabricated as follows. That is, a lead frame and window frame are fixed on a ceramic substrate via low-melting-point glass. After the CCD chip is fixed on the ceramic substrate, an electrode on the CCD chip, an inner lead, and an inner lead end portion having a recess are electrically connected by thin metal wires, and a cap is fixed via a thermosetting resin (see e.g., patent document 1).

Also, an integrated circuit die for an EPROM, CCD, and another optical IC device is fabricated as follows. This integrated circuit die has a substrate having metalized vias extending therethrough. The die is attached to the first surface of this substrate and electrically connected to the metalized vias. The substrate around this die is coated with an adhesive bead. The bead covers the side surfaces of the die, the peripheral portion of the first surface in the upper portion of the die, and bonding wires. A transparent encapsulating material layer is deposited on the die in a

cavity formed by the bead, and this encapsulating film is hardened, thereby forming the outer surface of the package (see e.g. patent document 2).

[0003]

[Patent Document 1]

Jpn. Pat. Appln. KOKAI Publication No. 04-246852

(page 1, FIG. 1)

[Patent Document 2]

PCT National Publication No. 2001-516956 (page 1, FIG.1)

[0004]

[Objects of the Invention]

The semiconductor package of the former prior art has a problem of a large thickness because external leads are included. The semiconductor package of the latter prior art has a problem in that since it has a substrate having metalized vias extending therethrough, that is, the substrate has a both side wiring construction and a through hole conducting portions, it is difficult to form the through hole conducting portions, and particularly if the substrate is a glass substrate, the formation of the through hole conducting portions is more difficult. In addition, the productivity is low because dies are mounted one by one on the substrate.

It is an object of the present invention to provide a semiconductor package which has no via hole conducting portion and can be made thin, and a method of fabricating the same.

It is another object of the present invention to provide a semiconductor package fabrication method capable of fabricating a plurality of semiconductor packages at once.

[0005]

[Means for Achieving the Objects]

An invention of claim 1 characterized by comprising a semiconductor substrate including a device region on its one surface and a connecting pad around the device region, an outer substrate formed on one surface side of the semiconductor substrate, a distribution wire formed on the other surface side of the semiconductor substrate, and connecting means, partially formed around the semiconductor substrate, for electrically connecting the connecting pad and distribution wire.

The invention of claim 2 is, in the invention according to claim 1, characterized in that the connecting means includes a distribution wire extended to the other surface side of the semiconductor substrate.

Then invention of claim 3 is, in the invention according to claim 1 characterized in that the connecting means includes a connecting wire having one end portion connected to the connecting pad, and the other end portion extended outside the semiconductor substrate.

The invention of claim 4 is, in the invention according to claim 3, characterized in that the connecting wire includes a metal layer formed of plating .

The invention of claim 5 is, in the invention according to claim 3, characterized in that the connecting wire includes a portion in close contact with one surface of the semiconductor substrate.

The invention of claim 6 is, in the invention according to claim 3, characterized in that the connecting wire is formed

in close contact with the support substrate.

The invention of claim 7 is, in the invention according to claim 3, characterized by comprising a projecting connecting electrode between the connecting pad and connecting wire.

The invention of claim 8 is, in the invention according to claim 3, characterized in that an insulating film is formed between the other surface of the semiconductor substrate, which includes the connecting wire extended outside the semiconductor substrate, and the distribution wire.

The invention of claim 9 is, in the invention according to claim 2, characterized in that the connecting means includes a connecting wire formed on the surface of the support substrate, which opposes the semiconductor substrate, and having one end portion connected to the connecting pad, and the other end portion extended outside the semiconductor substrate, and a columnar electrode formed on the other end portion of the connecting wire, and the distribution wire is connected to the columnar electrode.

The invention of claim 10 is, in the invention according to claim 9, characterized in that an insulating film is formed between the other surface of the semiconductor substrate, which includes the connecting wire extended outside the semiconductor substrate and the columnar electrode, and the distribution wire.

The invention of claim 11 is, in the invention according to claim 2, characterized in that the external electrode is formed on a connecting pad portion of the distribution wire, and an insulating film is so formed as to cover the other

surface of the semiconductor substrate, which includes the distribution wire except for the external electrode.

The invention of claim 12 is, in the invention according to claim 11, characterized in that the external electrode has a columnar electrode, and a solder ball is formed on the columnar external electrode.

The invention of claim 13 is, in the invention according to claim 1, characterized in that the device region is a photoelectric conversion device region.

The invention of claim 14 is, in the invention according to claim 1, characterized in that the support substrate is a glass substrate.

The invention of claim 15 is, in the invention according to claim 14, characterized in that a transparent adhesive layer or transparent encapsulating layer is provided between the semiconductor substrate and glass substrate.

An invention of claim 16 is characterized by comprising the steps of:

forming a plurality of connecting wires on one surface of a wafer-like semiconductor substrate including, on one surface, a plurality of device regions and a plurality of connecting pads each connected to one of said plurality of device regions, such that one end portion of each of said plurality of connecting wires is connected to the corresponding one of the connecting pads, and the other end portion of the connecting wire is extended outside the corresponding connecting pad;

placing a support substrate on the surface of the semiconductor substrate, which includes said plurality of

connecting wires;

exposing the other end portions of said plurality of connecting wires by removing, between the device regions, at least portions of the semiconductor substrate, which correspond to the other end portions of said plurality of connecting wires;

forming an external electrode electrically connected to the other end portion of each connecting electrode; and

obtaining a plurality of semiconductor packages each including the semiconductor substrate with the external electrode, by cutting the support substrate between the device regions.

The invention of claim 17 is, in the invention according to claim 16, characterized by comprising a step of thinning the semiconductor substrate by polishing the other surface of the semiconductor substrate, before at least portions of the semiconductor substrate, which correspond to the other end portions of said plurality of connecting wires are removed between the device regions.

An invention of claim 18 is characterised by comprising the steps of:

forming connecting wires each extending to a periphery of the inside of each of a plurality of semiconductor mounting regions from an inside of the semiconductor mounting region on one surface of a supporting substrate having a size corresponding to each of a plurality of semiconductor packages, and forming a columnar electrode on the connecting wire formed on the periphery of each of the semiconductor mounting region;

placing, on the semiconductor mounting region of the support substrate, a semiconductor substrate including a device region on a surface opposite to the support substrate and a connecting electrode around the device region, and connecting the connecting electrode of each semiconductor substrate to the connecting wire formed on the periphery of the inside of the semiconductor mounting region of the corresponding support substrate;

forming an external electrode electrically connected to each columnar electrode; and

obtaining a plurality of semiconductor packages, each having the semiconductor substrate provided with the external electrode, by cutting the supporting substrate between the semiconductor substrates.

The invention of claim 19 is, in the invention according to claim 18, characterized in that after the semiconductor substrate is placed on the semiconductor supporting region of the support substrate, an insulating film is so formed as to cover the other surface of the semiconductor substrate, which includes the columnar electrode, and polishing the surface of the insulating film and the other surface of the semiconductor substrate, thereby thinning the semiconductor substrate and exposing an upper surface of the columnar electrode.

The invention of claim 20 is, in the invention according to any one of claims 16 to 18, characterized in that the external electrode is formed on a distribution wire formed to be extended to a side of the other surface of the semiconductor substrate.

The invention of claim 21 is, in the invention according to claim 20, characterized by comprising a step of forming the external electrode on a connecting pad portion of the distribution wire, and a step of forming an insulating film so as to cover the other surface of the semiconductor substrate, which includes the distribution wire except for the external electrode.

The invention of claim 22 is, in the invention according to claim 21, characterized by comprising a step of forming a solder ball on the external electrode.

The invention of claim 23 is, in the invention according to any one of claims 16 to 18, characterized in that the device region is a photoelectric conversion device region.

The invention of claim 24 is, in the invention according to any one of claims 16 to 18, characterized in that the support substrate is a glass substrate.

The invention of claim 25 is, in the invention according to claim 24, characterized by comprising a step of forming a transparent adhesive layer or transparent encapsulating film between the semiconductor substrate and glass substrate.

In the present invention, a semiconductor substrate has a device region on its one surface and has connecting pads around this device region. An outer substrate is formed on this surface of the semiconductor substrate, and distribution wires are formed on the other surface. This makes it possible to decrease the thickness of the obtained semiconductor package. In addition, a portion of a connecting means for connecting each connecting pad to the distribution wire is formed around

the semiconductor substrate. Accordingly, no through hole conducting portion is necessary. Also, since the connecting means and distribution wires can be sequentially formed on a plurality of semiconductor substrates, the productivity can be increased.

[0006]

[Embodiments of the Invention]

(First Embodiment)

FIG. 1 shows a sectional view of a semiconductor package according to the first embodiment of the present invention. This semiconductor package includes a silicon substrate (semiconductor substrate) 1. In a central portion of the lower surface of the silicon substrate 1, a photoelectric conversion device region 2 including an element such as a CCD, photodiode, or phototransistor is formed.

[0007]

In a peripheral portion of the lower surface of the silicon substrate 1, a plurality of connecting pads 3 made of an aluminum-based metal or the like are formed to be electrically connected to the photoelectric conversion device region 2. An insulating film 4 made of silicon oxide or the like is formed on that lower surface of the silicon substrate 1, which includes the lower surface of the device region 2, except for central portions of the connecting pads 3. These central portions of the connecting pads 3 are exposed through holes 5 formed in the insulating film 4.

[0008]

An insulating film 6 made of polyimide or the like is

formed on the upper surface and side surfaces of the silicon substrate 1. In this structure, the lowest surface of the insulating film 6 formed on the side surfaces of the silicon substrate 1 is substantially leveled with the lower surface of the insulating film 4 formed on the lower surface of the silicon substrate 1.

[0009]

From the lower surface of each connecting pad 3 exposed through the hole 5 in the insulating film 4 to a predetermined portion of the lower surface of the insulating film 6 formed around the connecting pad 3, a connecting wire 7 made of a first metal layer or base layer 7a and a second metal layer or a main layer 7b formed below the first metal layer 7a is formed. As a consequence, one end portion of each connecting wire 7 is connected to the connecting pad 3 of the silicon substrate 1. The other end portion of the wire 7 extends outside the silicon substrate 1.

[0010]

On those lower surfaces of the silicon substrate 1 and the insulating film 6, which include the connecting wires 7, a glass substrate 9 as a support substrate is formed via a transparent adhesive layer 8 made of a transparent epoxy-based resin. Accordingly, the dimension in the lateral direction of the glass substrate 9 is slightly larger than that of the silicon substrate 1.

[0011]

In that portion of the insulating film 6, which corresponds to the other end portion of each connecting wire 7,

a hole 10 is formed. From the upper surface of the other end portion of each connecting wire 7 exposed through the hole 10 to a predetermined portion of the upper surface of the insulating film 6, a distribution wire 11 made of a lower metal layer 11a and an upper metal layer 11b formed on the lower metal layer 11a is formed.

[0012]

A columnar electrode (external electrode) 12 is formed on the upper surface of that connecting pad portion of each distribution wire 11. On the upper surface of the insulating film 6 including the distribution wires 11, an encapsulating film (insulating film) 13 made of an epoxy-based resin or the like is formed such that its upper surface is substantially leveled with the upper surface of each columnar electrode 12. A solder ball 14 is formed on the upper surface of each columnar electrode 12.

[0013]

An example of a method of fabricating this semiconductor package will be described below. First, as shown in FIG. 2, a structure is prepared in which photoelectric conversion device regions 2, aluminum connecting pads 3, and a silicon oxide insulating film 4 are formed on a wafer-like silicon substrate (semiconductor substrate) 1, and a central portion of each connecting pad 3 is exposed through a hole 5 formed in the insulating film 4. The thickness of the silicon substrate 1 in this state is larger to a certain extent than that shown in FIG. 1.

[0014]

Next, as shown in FIG. 3, a first metal layer 7a is formed on the entire upper surface of the insulating film 4, which includes the upper surfaces of the connecting pads 3 exposed through the holes 5. In this example, the first metal layer 7a is made only of a copper layer formed by electroless plating. However, the metal layer 7a may also be made only of a copper layer formed by sputtering, or obtained by forming a copper layer by sputtering on a thin layer of titanium or the like formed by sputtering. This similarly applies to a lower metal layer 11a (to be described later).

[0015]

A plating resist layer 21 is pattern-formed on the upper surface of the first metal layer 7a. Holes 22 are formed in those portions of the plating resist film 21, which correspond to regions where connecting wires 7 are to be formed. The first metal layer 7a is then used as a plating electric current path to perform electroplating of copper, thereby forming a second metal layer 7b on the upper surface of the first metal layer 7a in each hole 22 of the plating resist film 21.

[0016]

Subsequently, the plating resist film 21 is removed, and the second metal layer 7b is used as a mask to etch away unnecessary portions of the first metal layer 7a, so that, as shown in FIG. 4, the first metal layer 7a remains only below the second metal layer 7b, forming connecting wires 7 each made of the remaining first metal layer 7a and the second metal layer 7b formed on the entire upper surface of the first metal

layer 7a.

[0017]

As shown in FIG. 5, a glass substrate 9 is adhered to the entire upper surface of the insulating film 4, which includes the connecting wires 7, via a transparent adhesive layer 8 made of an epoxy-based resin or the like. This structure shown in FIG. 5 is then turned upside down. As shown in FIG. 6, the silicon substrate 1 is thinned by properly polishing the upper surface of the silicon substrate 1 away from the surface on which the photoelectric conversion device regions 2 are formed. For example, the thickness of the silicon substrate 1 is decreased to 50 μm.

[0018]

Subsequently, of the portions of the wafer-sized silicon substrate 1, unnecessary portions not corresponding to the silicon substrate shown in FIG. 1, and the insulating film 4 on the lower surface thereof are removed by dicing, etching, or the like, as shown in FIG. 7. Accordingly, in this state, the upper surfaces of the transparent adhesive layer 8 and the connecting wire 7 disposed around the silicon substrate 1 are exposed, and the exposed surfaces are

are substantially leveled with the lower surface of the insulating film 4.

[0019]

As shown in FIG. 8, an insulating film 6 made of photosensitive polyimide or the like is formed by patterning on the entire upper surface of the silicon substrate 1, which includes the connecting wires 7 formed around the silicon

substrate 1 and the transparent adhesive layer 8. In this structure, holes 10 are formed in those portions of the insulating film 6, which correspond to the other end portions of the connecting wires 7.

[0020]

As shown in FIG. 9, a lower metal layer 11a is formed by electroless plating on the entire upper surface of the insulating film 6, which includes the other end portions of the connecting wires 7 exposed through the holes 10. A plating resist film 23 is then formed on the upper surface of the lower metal layer 11a by patterning. In this structure, holes 24 are formed in those portions of the plating resist film 23, which correspond to regions where distribution wires 11 are to be formed. Subsequently, electroplating of copper is performed by using the lower metal layer 11a as a plating electric current path, thereby forming an upper metal layer 11b on the upper surface of the lower metal layer 11a in each hole 24 of the plating resist film 23. After that, the plating resist film 23 is peeled.

[0021]

As shown in FIG. 10, a plating resist film 25 is formed on the upper surfaces of the upper metal layer 7b and lower metal layer 7a. In this structure, holes 26 are formed in those portions of the plating resist film 25, which correspond to regions where columnar electrodes 12 are to be formed. Electroplating of copper is then performed by using the lower metal layer 11a as a plating electric current path, thereby forming a columnar electrode 12 on the upper surface of a

connecting pad portion of the upper metal layer 11b in each hole 26 of the plating resist film 25.

[0022]

The plating resist film 25 is peeled, and unnecessary portions of the lower metal layer 11a are etched away by using the columnar electrodes 12 and upper metal layer 11b as masks. Consequently, as shown in FIG. 11, the lower metal layer 11a remains only below the upper metal layer 11b, forming distribution wires 11 each made of the remaining lower metal layer 11a and the upper metal layer 11b formed on the entire upper surface of the lower metal layer 11a.

[0023]

As shown in FIG. 12, on the entire upper surface of the insulating film 6, which includes the columnar electrodes 12 and distribution wires 11, an encapsulating film 13 made of an epoxy-based resin is formed such that its thickness is larger than the height of the columnar electrodes 12. In this state, therefore, the upper surface of each columnar electrode 12 is covered with the encapsulating film 13. The upper surfaces of the encapsulating film 13 and columnar electrodes 12 are then properly polished. Consequently, as shown in FIG. 13, the upper surface of each columnar electrode 12 is exposed, and the upper surface of the encapsulating film 13, which includes these exposed upper surfaces of the columnar electrodes 12 is planarized.

[0024]

As shown in FIG. 14, a solder ball 14 is formed on the upper surface of each columnar electrode 12. To assure the

bonding strength between the columnar electrode 12 and solder ball 14, before the formation of the solder balls 14 it is also possible to etch away burrs formed on the surfaces of the columnar electrodes 12, perform plating for preventing oxidation, or perform a pretreatment such as flux coating. By this pretreatment, the upper surface of each columnar electrode 12 and the upper surface of the encapsulating film 13 can be kept substantially leveled with each other, even if slight unevenness is produced between them.

[0025]

Finally, as shown in FIG. 15, the encapsulating film 13, insulating film 6, transparent adhesive layer 8, and glass substrate 9 are cut between the adjacent silicon substrates 1. As a consequence, a plurality of semiconductor packages shown in FIG. 1 are obtained.

[0026]

In the thus obtained semiconductor package, the glass substrate 9 as an outer substrate is formed via the transparent adhesive layer 8 on that surface of the silicon substrate 1, on which the photoelectric conversion device 2 is formed. On the surface of the silicon substrate 1 away from the surface on which the photoelectric conversion device 2 is formed, the insulating film 6, distribution wires 11, columnar electrodes 12, encapsulating film 13, and solder balls 14 are formed. Accordingly, the semiconductor package can be made thinner than when external leads are formed.

[0027]

Also, the other end portion of each connecting wire 7 for

electrically connecting the connecting pad 3 of the silicon substrate 1 and the distribution wire 11 is formed around the silicon substrate 1. Therefore, no through hole conducting portion need be formed.

[0028]

In addition, this semiconductor package has the columnar electrodes 12. Therefore, after the semiconductor package is mounted on a circuit board (not shown) via the solder balls 14, the stress caused by the thermal expansion coefficient difference between the silicon substrate 1 and circuit board can be reduced to some extent by the columnar electrodes 12.

[0029]

Furthermore, in the above fabrication method, the formation of the connecting wires 7, the adhesion of the glass substrate 9 via the transparent adhesive layer 8, and the formation of the insulating film 6, distribution wires 11, columnar electrodes 12, encapsulating film 13, and solder balls 14 are sequentially performed on the silicon substrate 1 in the form of a wafer. Since the resultant structure is cut into a plurality of semiconductor packages after that, the productivity increases.

[0030]

In the first embodiment described above, the connecting wires 7 to be connected to the connecting pads 3 formed in the silicon substrate 1 having the photoelectric conversion device region 2 are formed by using the silicon substrate 1 as a base member. However, it is also possible to form the connecting wires 7 on the glass substrate 9 in advance, and connect the

connecting pads 3 formed in the silicon substrate 1 having the photoelectric conversion device region 2 to the connecting wires 7. An embodiment of this method will be described below.

[0031]

(Second Embodiment)

FIG. 16 is a sectional view of a semiconductor package according to the second embodiment of the present invention. The main characteristic features of this semiconductor package are that a bump electrode (connecting electrode) 31 formed on a lower surface of a base metal layer 30 on a lower surface of a connecting pad 3 of a silicon substrate 1 is connected onto one end portion of a connecting wire 7. The connection wire 7 is made up of a first metal layer or base layer 7a and second metal layer or main layer 7b formed on a glass substrate 9. A transparent encapsulating film 32 made of a transparent epoxy-based resin or the like is formed between the silicon substrate 1 and glass substrate 9. A distribution wire 11, made up of a first metal layer 11a or base layer and second metal layer 11b or main layer is connected onto a columnar electrode 33 formed on the other end portion of each connecting wire 7. The connecting wires 7 and columnar electrodes 33 around the silicon substrate 1 are covered with an encapsulating film (insulating film) 34 made of an epoxy-based resin or the like.

[0032]

An example of a method of fabricating this semiconductor package will be described below. First, as shown in FIG. 17, on the upper surface of a glass substrate 9 having a size

corresponding to a plurality of semiconductor packages, preferably, a size equivalent to the wafer size as in the first embodiment, connecting wires 7 each made up of a first metal layer 7a and second metal layer 7b are formed to extend outward from positions corresponding to connecting pads 3 connected to a photoelectric conversion device region 2 formed on the wafer. Subsequently, a columnar electrode 33 is formed on the outside end of each connecting wire 7.

[0033]

The connecting wires 7 and columnar electrodes 33 can be formed by the method explained with reference to FIG. 3 (replace silicon substrate 1 with glass substrate 9) and FIG. 11. Referring to FIG. 17, between a pair of connecting wires 7 on each of which the columnar electrode 33 is formed, a silicon substrate mounting region in which a silicon substrate having the connecting pads 3 connected to the photoelectric conversion device region 2 is to be mounted is formed.

[0034]

As shown in FIG. 18, a silicon substrate 1 is mounted on each of a plurality of semiconductor substrate mounting regions of the glass substrate 9, and connected to the connecting wires 7. In this state, the photoelectric conversion device region 2, the connecting pads 3, and an insulating film 4 are formed on the silicon substrate 1. In addition, a base metal layer 30 and bump electrode 31 are formed on each connecting pad 3. The base metal layer 30 and bump electrode 31 can be formed by any already known method.

[0035]

The bump layer 31 formed in a peripheral portion of the lower surface of the silicon substrate 1 is connected to the connecting wires 7 formed in the perimeter of the silicon substrate mounting region. As in the first embodiment, the thickness of the silicon substrate 1 is larger to some extent than that in the semiconductor package shown in FIG. 16. Also, in this state, only a good product is used as the silicon substrate 1 including the photoelectric conversion device region 2 and the like. Then, an encapsulating film 32 made of a transparent epoxy-based resin is formed by filling the resin between the silicon substrate 1 and glass substrate 9.

[0036]

As shown in FIG. 19, the entire upper surface of the glass substrate 9, which includes the silicon substrate 1, connecting wires 7, and columnar electrodes 33 is covered with an encapsulating film 34 made of an epoxy-based resin. Then, the upper surfaces of the encapsulating film 34, silicon substrate 1, and columnar electrodes 33 are properly polished. Consequently, as shown in FIG. 20, the upper surfaces of the silicon substrate 1 and columnar electrodes 33 are exposed from the encapsulating film 34, the silicon substrate 1 is thinned, and the upper surface of the encapsulating film 34, which includes the exposed silicon substrate 1 and columnar electrodes 33 is planarized.

[0037]

Subsequently, as shown in FIG. 21, an insulating film 6 made of photosensitive polyimide or the like is formed by

patterning on the entire upper surface including the silicon substrate 1, columnar electrodes 33, and encapsulating film 34. In this structure, a hole 10 is formed in that portion of the insulating film 6, which corresponds to a central portion of the upper surface of each columnar electrode 33.

[0038]

By performing the fabrication steps shown in FIGS. 9 to 14, distribution wires 11 each made up of a first metal layer or base layer 11a and second metal layer or main layer 11b, columnar electrodes 12, encapsulating film 13, and solder balls 14 are formed as shown in FIG. 22. Each distribution wire 11 is connected to the upper surface of the columnar electrode 33 through the hole 10. Finally, as shown in FIG. 23, the encapsulating film 13, insulating film 6, encapsulating film 34, and glass substrate 9 are cut between the adjacent silicon substrates 1. As a consequence, a plurality of semiconductor packages shown in FIG. 16 are obtained.

[0039]

In the thus obtained semiconductor package, the glass substrate 9 as an outer substrate is formed via the transparent encapsulating film 32 on that surface of the silicon substrate 1, on which the photoelectric conversion device 2 is formed. On the surface of the silicon substrate 1 away from the surface on which the photoelectric conversion device 2 is formed, the insulating film 6, distribution wires 11, columnar electrodes 12, encapsulating film 13, and solder balls 14 are formed. Accordingly, the semiconductor package can be made thinner than when external leads are formed.

[0040]

Also, a portion of each connecting wire 7 for electrically connecting the connecting pad 3 of the silicon substrate 1 and the distribution wire 11, and each columnar electrode 33 are formed around the silicon substrate 1. Therefore, no through hole conducting portion need be formed in the supporting member.

[0041]

In addition, this semiconductor package has the columnar electrodes 12. Therefore, after the semiconductor package is mounted on a circuit board (not shown) via the solder balls 14, the stress caused by the thermal expansion coefficient difference between the silicon substrate 1 and circuit board can be reduced to some extent by the columnar electrodes 12.

[0042]

Furthermore, in the above fabrication method, the formation of the connecting wires 7 and columnar electrodes 33, the mounting of the silicon substrate 1, and the formation of the transparent encapsulating film 32, encapsulating film 34, insulating film 6, distribution wires 11, columnar electrodes 12, encapsulating film 13, and solder balls 14 are sequentially performed on the glass substrate 9 having a size corresponding to a plurality of semiconductor packages. Since the resultant structure is cut into a plurality of semiconductor packages after that, the productivity can be increased.

[0043]

(Other Embodiments)

In each of the above embodiments, the solder ball 14 is

formed on the columnar electrode 12 formed on the connecting pad portion of the distribution wire 11. However, the present invention is not limited to these embodiments. For example, as in another embodiment of the present invention shown in FIG. 24, an insulating film 42 having holes 41 in portions corresponding to connecting pad portions of distribution wires 11 may be formed by patterning on the entire upper surface of an insulating film 6, which includes the distribution wires 11. In this structure, a solder ball 14 is formed in and on each hole 42 so as to be connected to the connecting pad portion of the distribution wire 11.

[0044]

Also, in each of the above embodiments, a photoelectric conversion device is formed on a semiconductor substrate. However, the present invention is applicable not only to a photoelectric conversion device but also to an integrated circuit for a memory or for control, or to a device in which a sensor element or the like is formed.

[0045]

[Advantages of the Invention]

As described above, in the present invention, a semiconductor substrate has a device region on its one surface and has connecting pads around this device region. An outer substrate is formed on this surface of the semiconductor substrate, and distribution wires are formed on the other surface. This makes it possible to decrease the thickness of the obtained semiconductor package. In addition, a portion of a connecting means for connecting each connecting pad to the

distribution wire is formed around the semiconductor substrate. Accordingly, no through hole conducting portion is necessary. Also, since the connecting means and distribution wires can be sequentially formed on a plurality of semiconductor substrates, the productivity can be increased.

[Brief Description of the Drawings]

[FIG. 1]

A sectional view of a semiconductor package according to the first embodiment of the present invention.

[FIG. 2]

A sectional view showing an initially prepared structure in an example of a method of fabricating the semiconductor package shown in FIG. 1.

[FIG. 3]

A sectional view for explaining a fabrication step following FIG. 2.

[FIG. 4]

A sectional view for explaining a fabrication step following FIG. 3.

[FIG. 5]

A sectional view for explaining a fabrication step following FIG. 4.

[FIG. 6]

A sectional view for explaining a fabrication step following FIG. 5.

[FIG. 7]

A sectional view for explaining a fabrication step following FIG. 6.

[FIG. 8]

A sectional view for explaining a fabrication step following FIG. 7.

[FIG. 9]

A sectional view for explaining a fabrication step following FIG. 8.

[FIG. 10]

A sectional view for explaining a fabrication step following FIG. 9.

[FIG. 11]

A sectional view for explaining a fabrication step following FIG. 10.

[FIG. 12]

A sectional view for explaining a fabrication step following FIG. 11.

[FIG. 13]

A sectional view for explaining a fabrication step following FIG. 12.

[FIG. 14]

A sectional view for explaining a fabrication step following FIG. 13.

[FIG. 15]

A sectional view for explaining a fabrication step following FIG. 14.

[FIG. 16]

A sectional view of a semiconductor package according to the second embodiment of the present invention.

[FIG. 17]

A sectional view showing an initial fabrication step in an example of a method of fabricating the semiconductor package shown in FIG. 16.

[FIG. 18]

A sectional view for explaining a fabrication step following FIG. 17.

[FIG. 19]

A sectional view for explaining a fabrication step following FIG. 18.

[FIG. 20]

A sectional view for explaining a fabrication step following FIG. 19.

[FIG. 21]

A sectional view for explaining a fabrication step following FIG. 20.

[FIG. 22]

A sectional view for explaining a fabrication step following FIG. 21.

[FIG. 23]

A sectional view for explaining a fabrication step following FIG. 22.

[FIG. 24]

A sectional view of a semiconductor package according to still another embodiment of the present invention.

[Explanation of Reference Symbols]

1 Silicon substrate

2 Photoelectric conversion device region

3 Connecting pad

4 Insulating film

6 Insulating film

7 Connecting wire

8 Transparent adhesive layer

9 Glass substrate

11 Distribution wire

12 Columnar electrode

13 Encapsulating film

14 Solder ball

31 Bump electrode

32 Encapsulating film

33 Columnar electrode

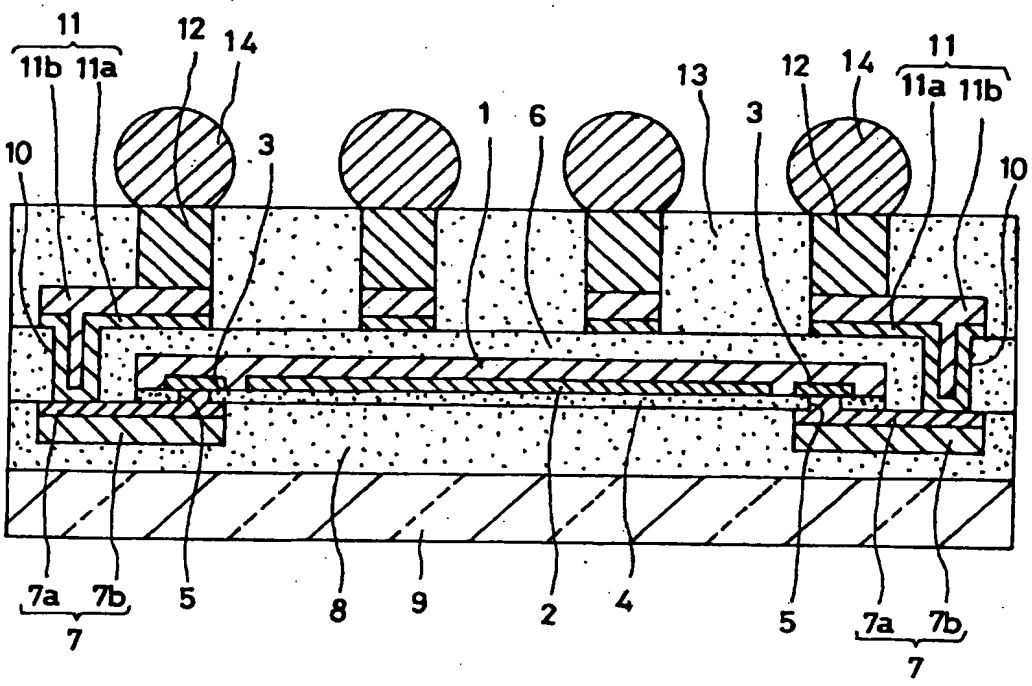
34 Encapsulating film

NAME OF DOCUMENT

【書類名】　図面　DRAWINGS

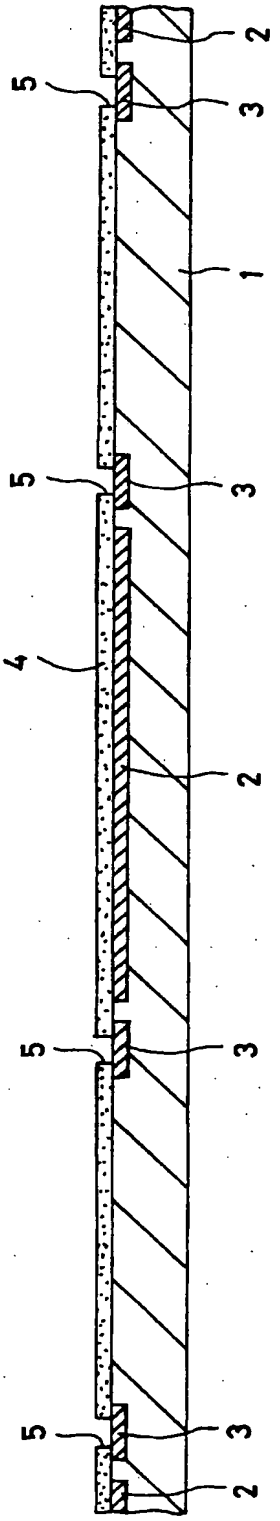
【図１】

FIG. 1



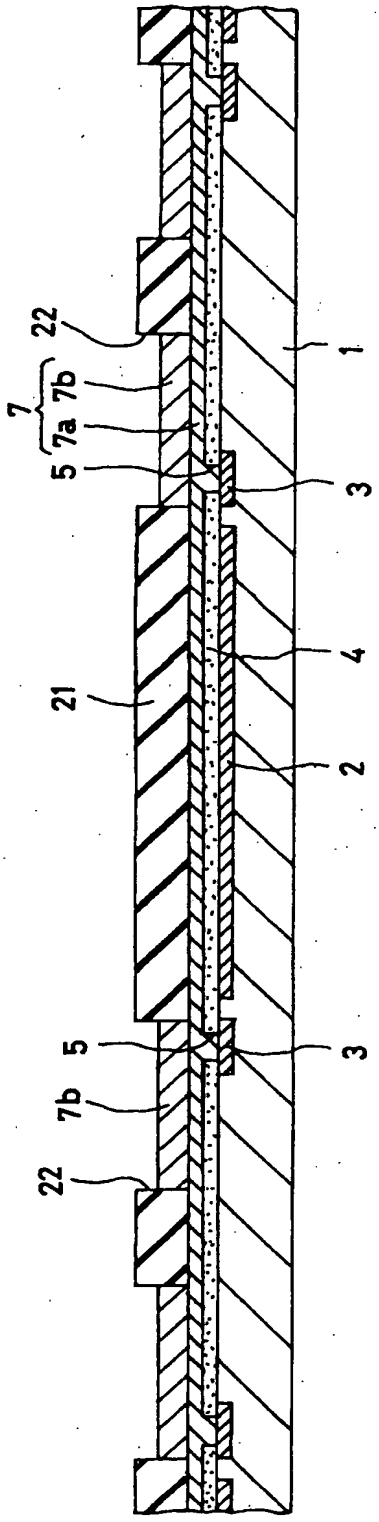
【図２】

FIG. 2



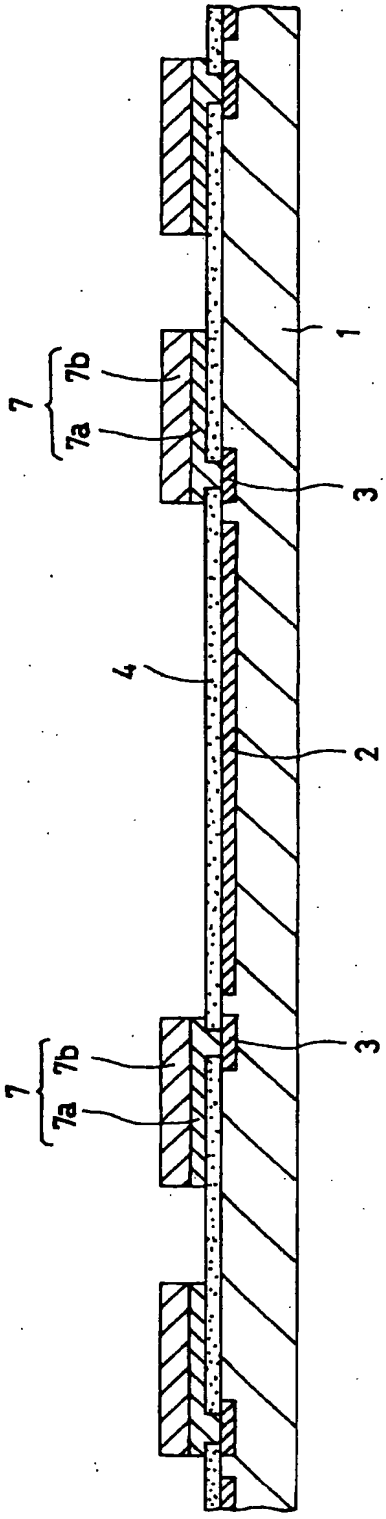
【図３】

FIG. 3



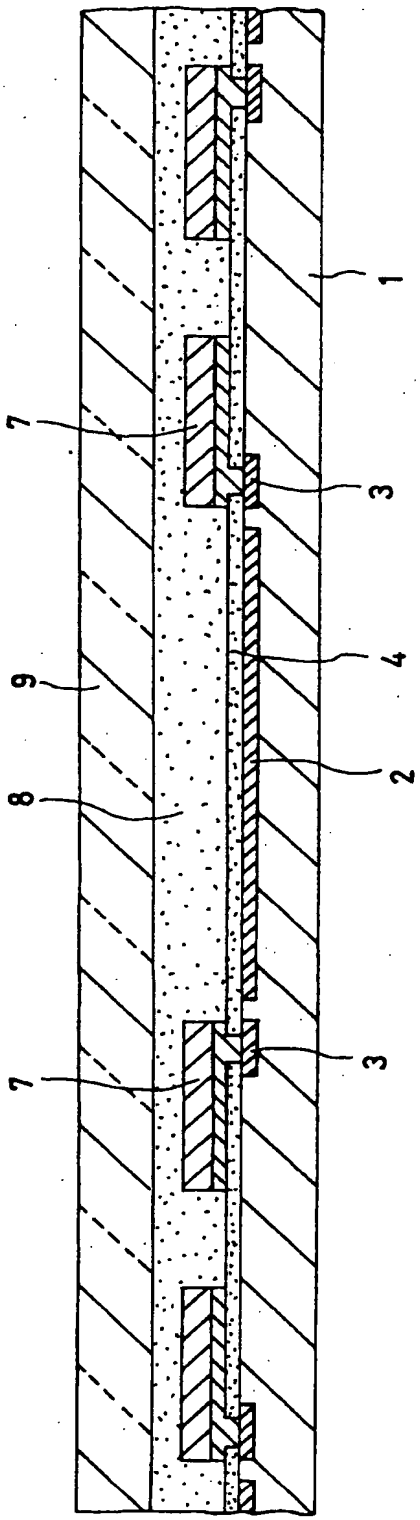
【図４】

FIG. 4



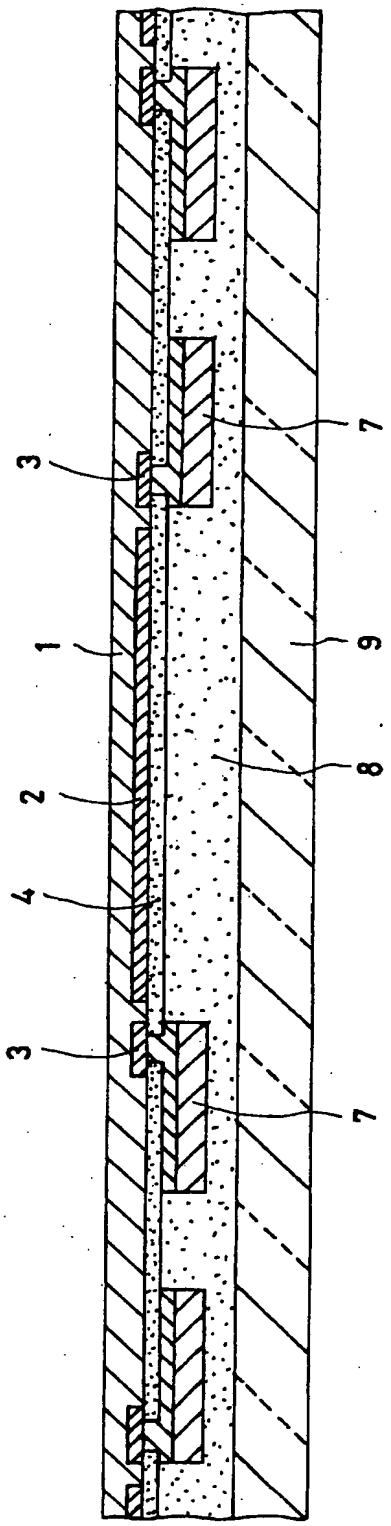
【図５】

FIG. 5



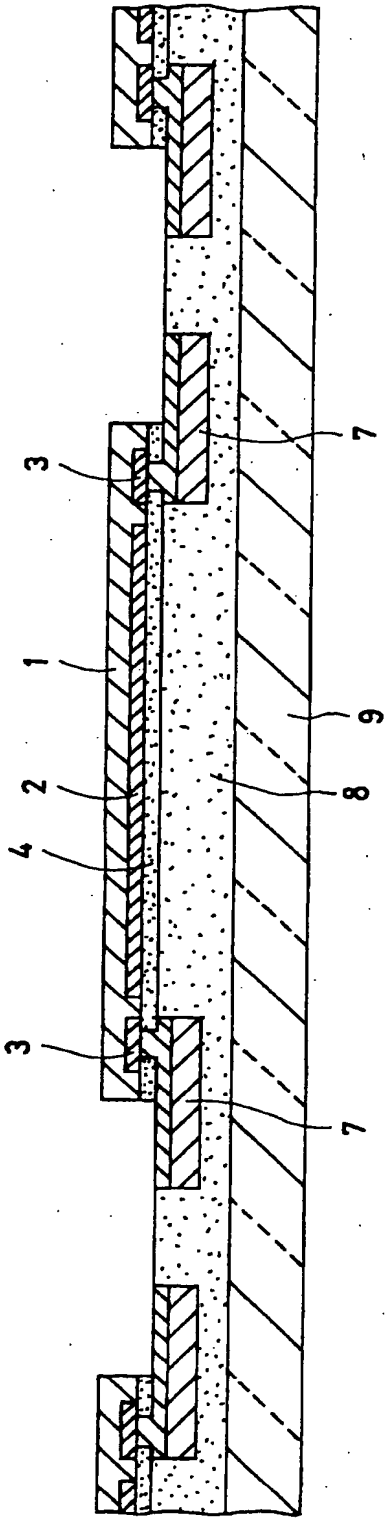
【図6】

FIG. 6



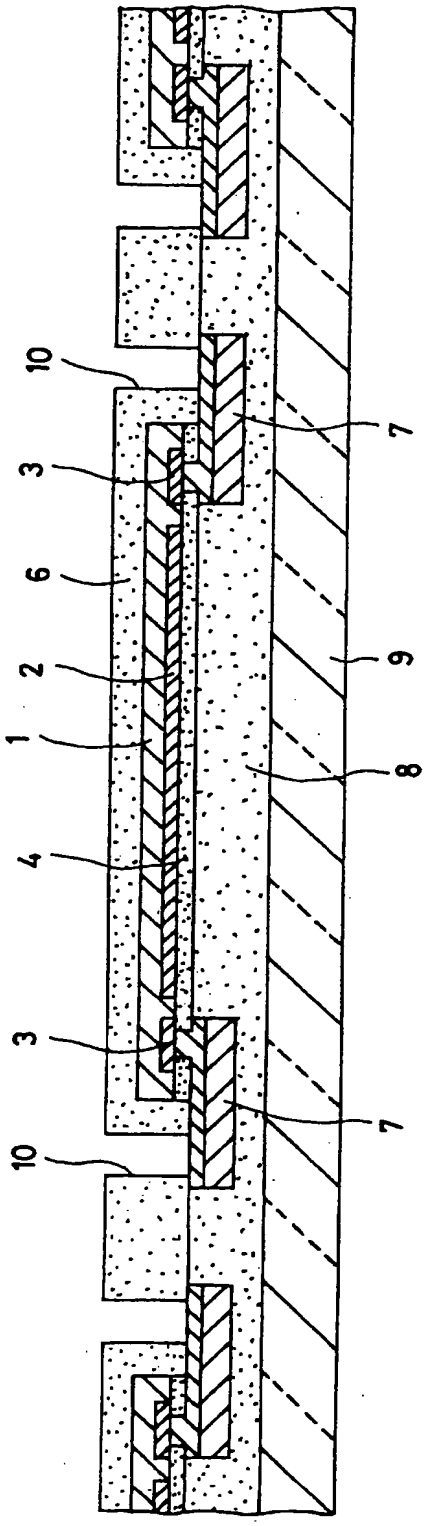
【図7】

FIG. 7



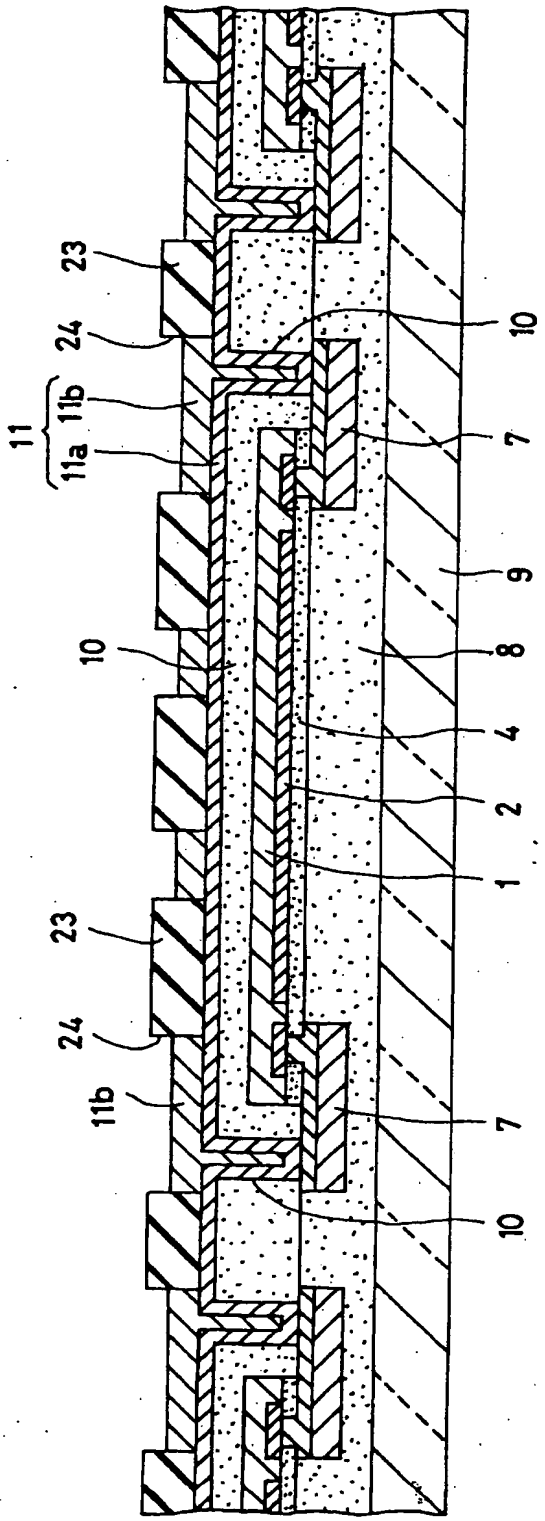
【図８】

FIG. 8



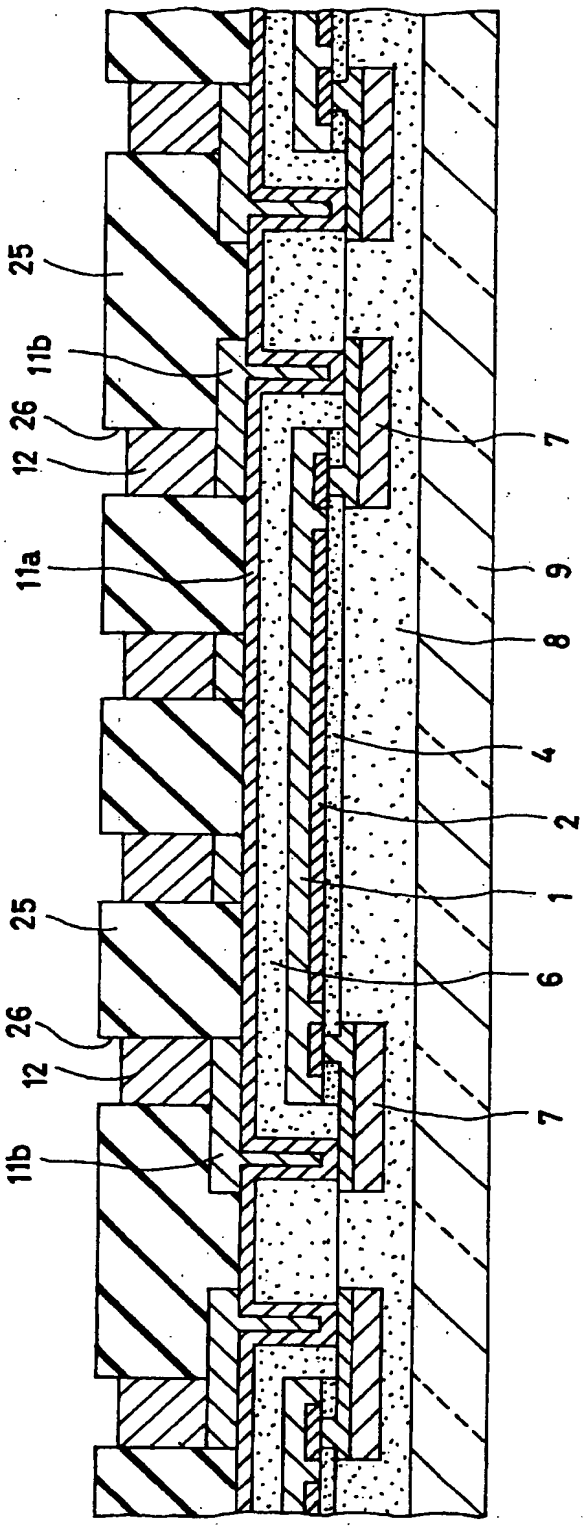
【図９】

FIG. 9



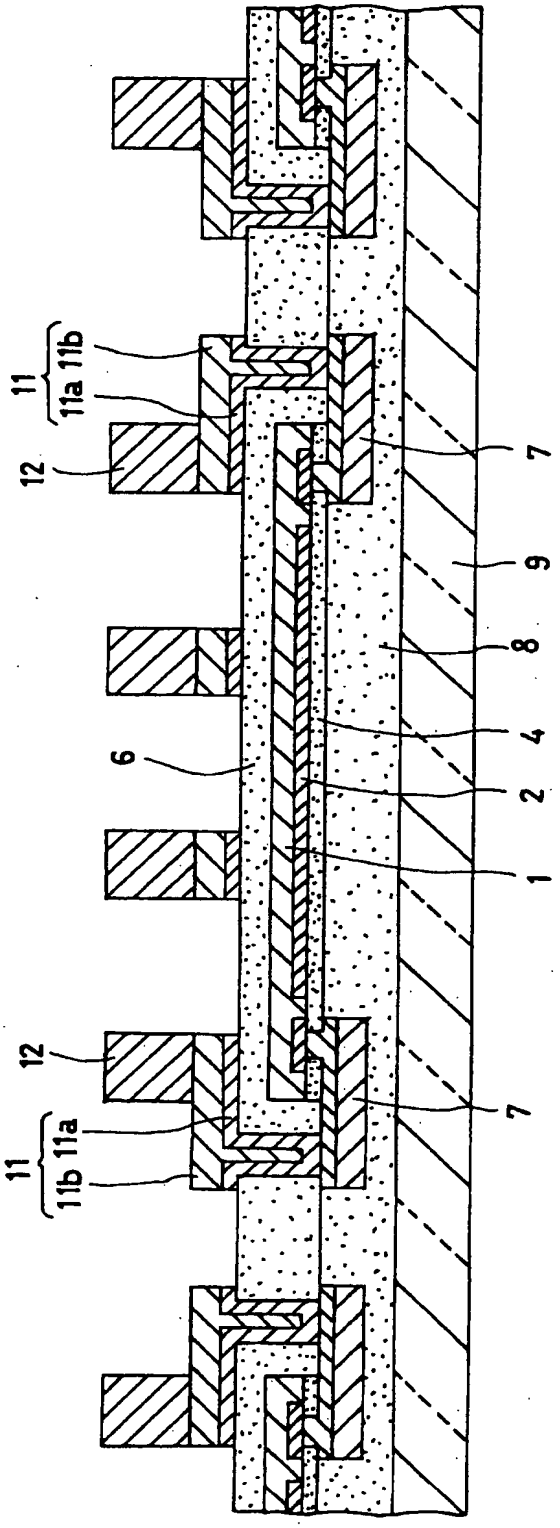
【図１０】

FIG. 10



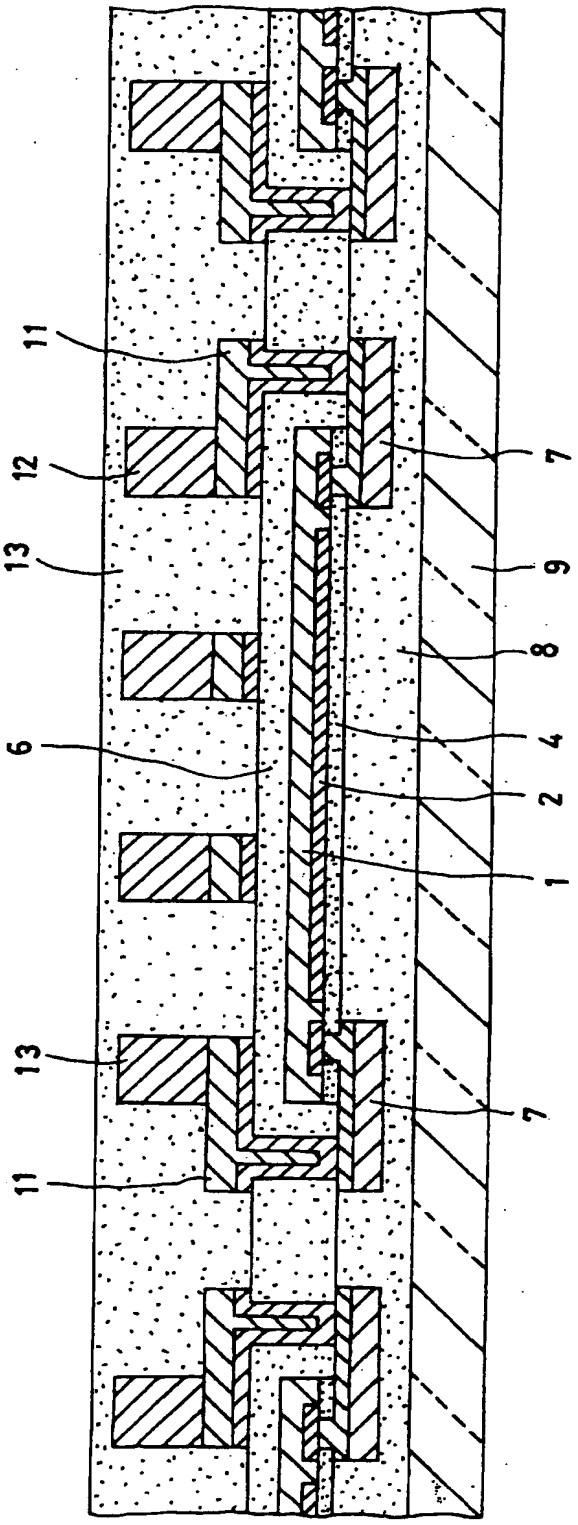
【図１１】

FIG. 11



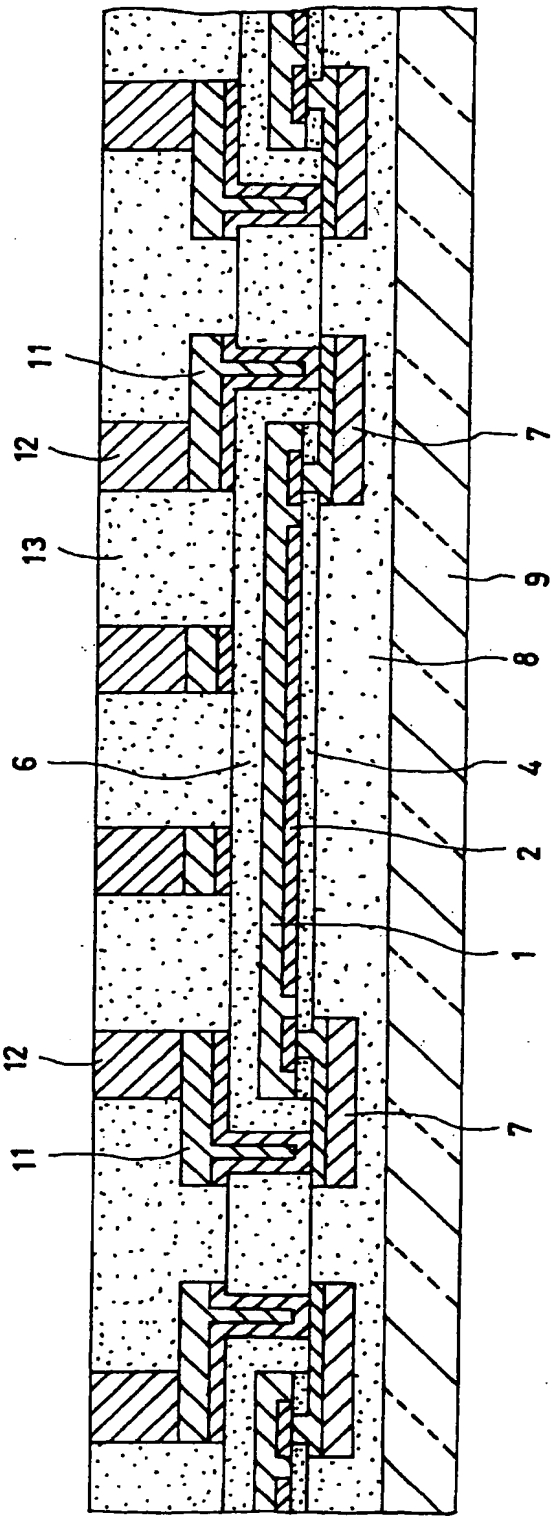
【図１２】

FIG. 12



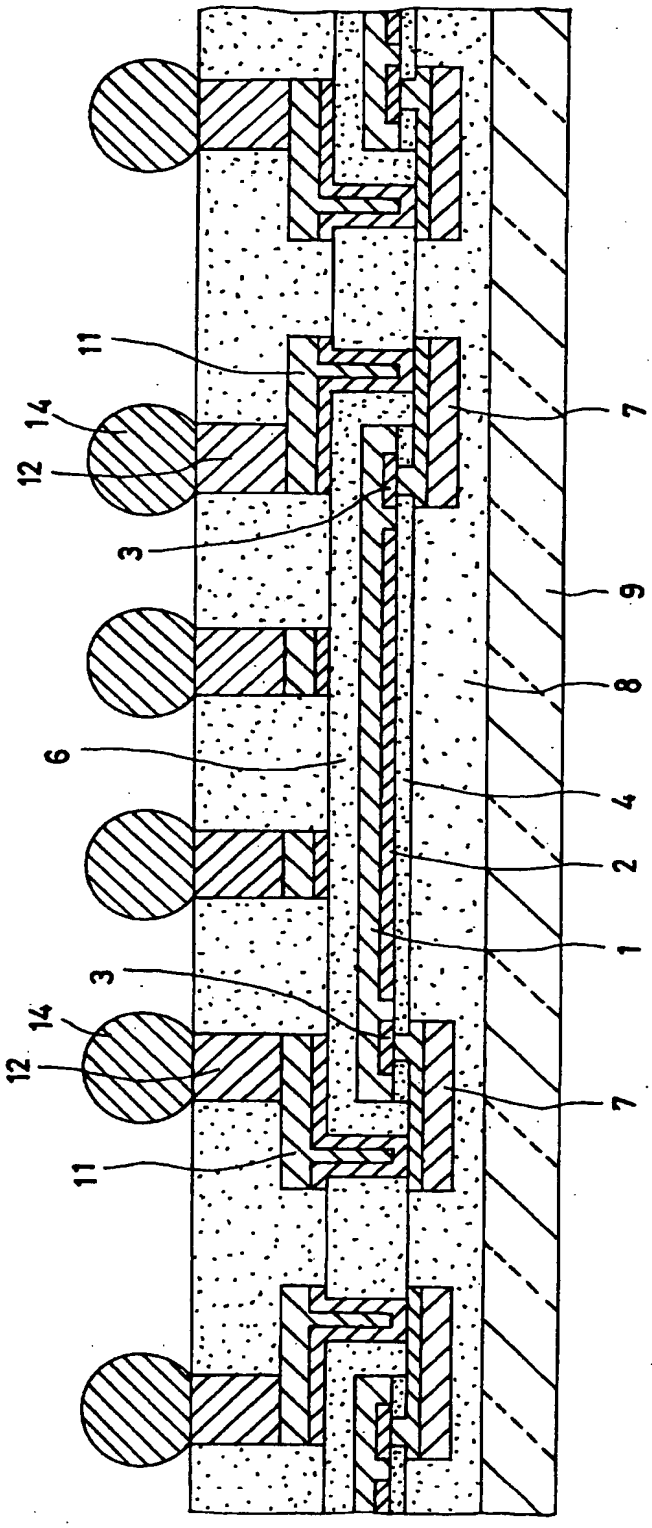
【図１３】

FIG. 13



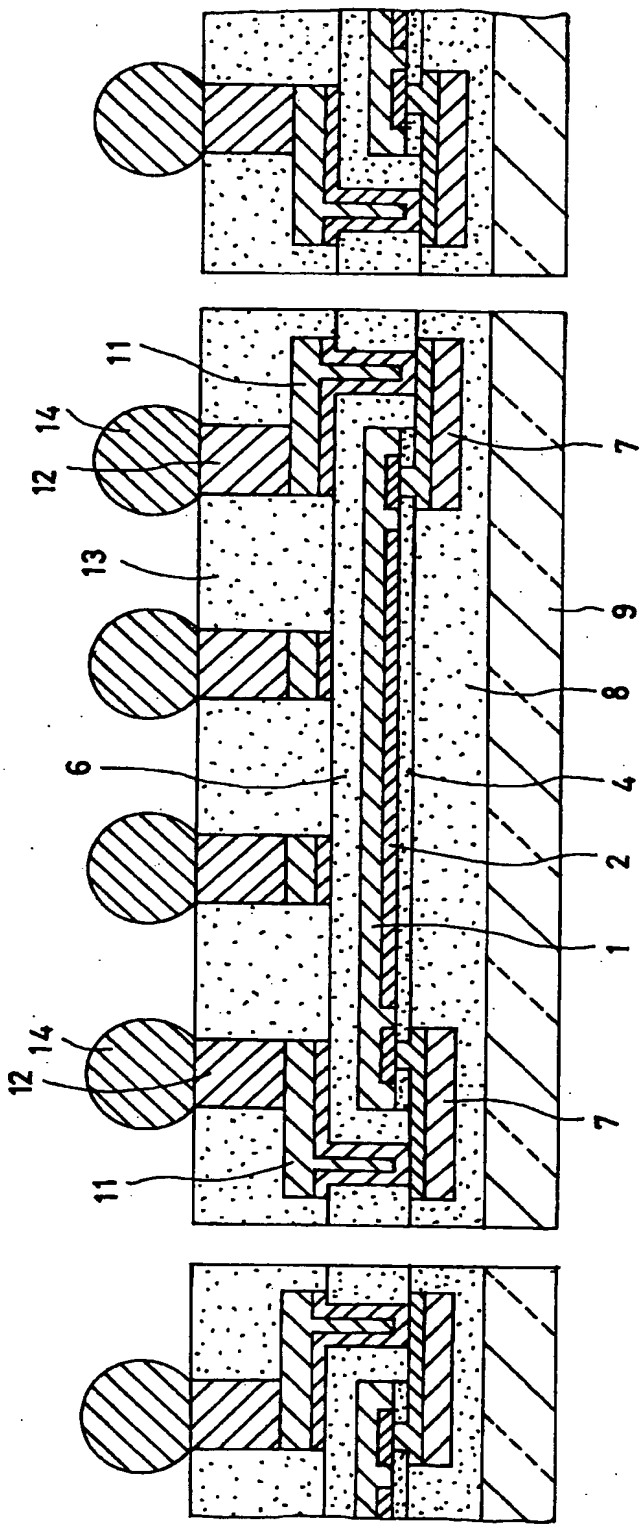
【図１４】

FIG. 14



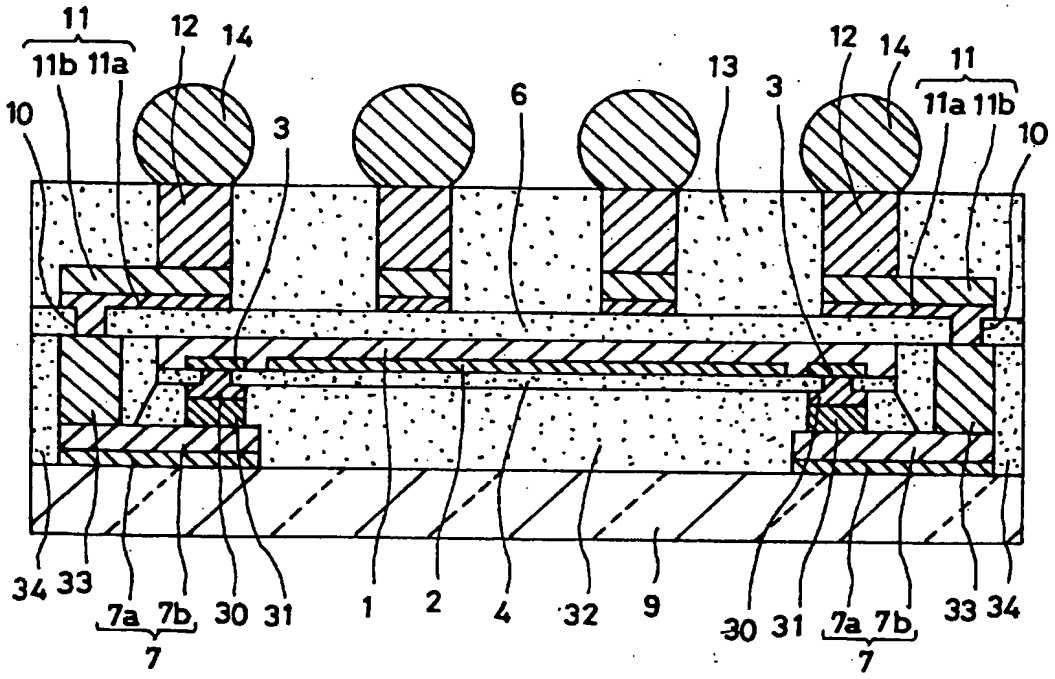
【図１５】

FIG. 15



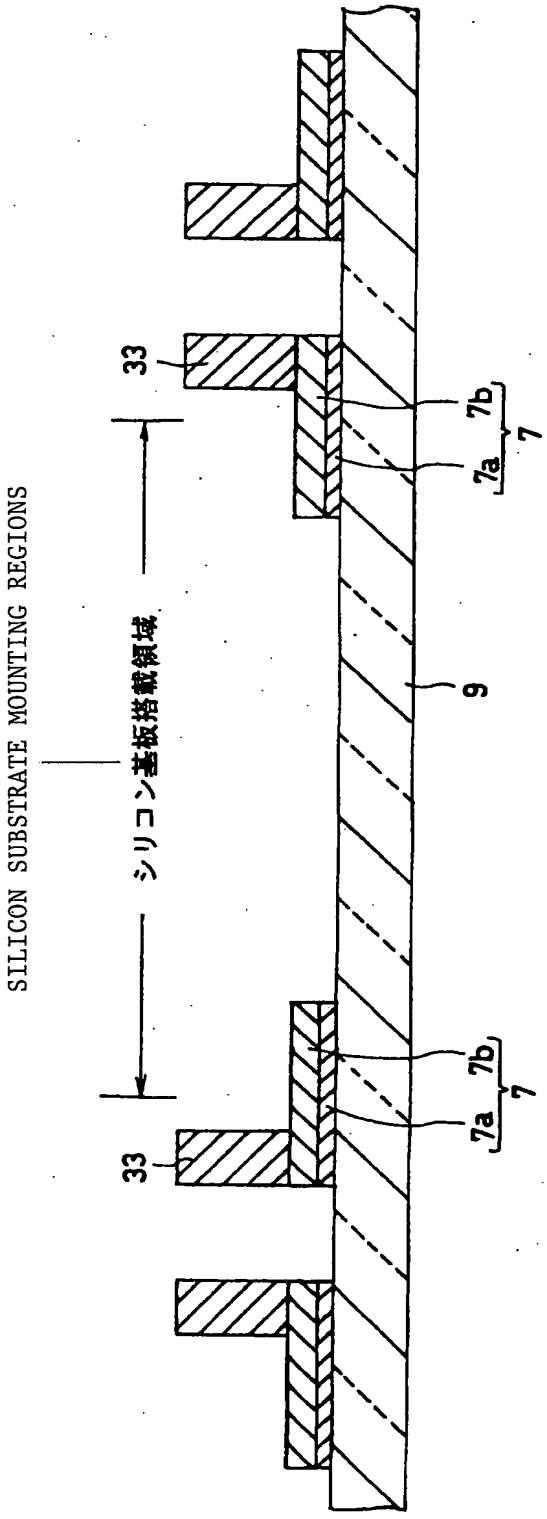
【図１６】

FIG. 16


11
11b 11a
12
14
10
3
6
13
3
12
14
11
11a 11b
10
34 33
7a 7b
7
30 31
1
2
4
32
9
30 31
7a 7b
7
33 34

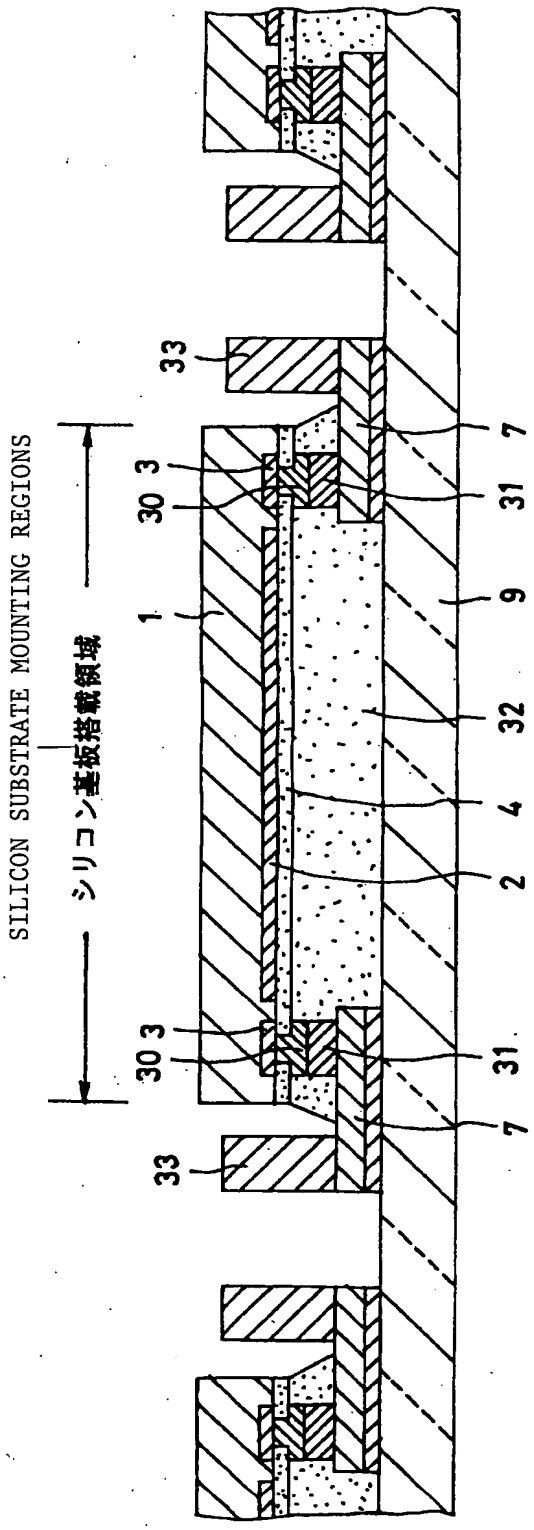
【図１７】

FIG. 17


SILICON SUBSTRATE MOUNTING REGIONS
シリコン基板搭載領域
33
33
7b
7a
7
7b
7a
7
9

【図１８】

FIG. 18


SILICON SUBSTRATE MOUNTING REGIONS
シリコン基板搭載領域
33
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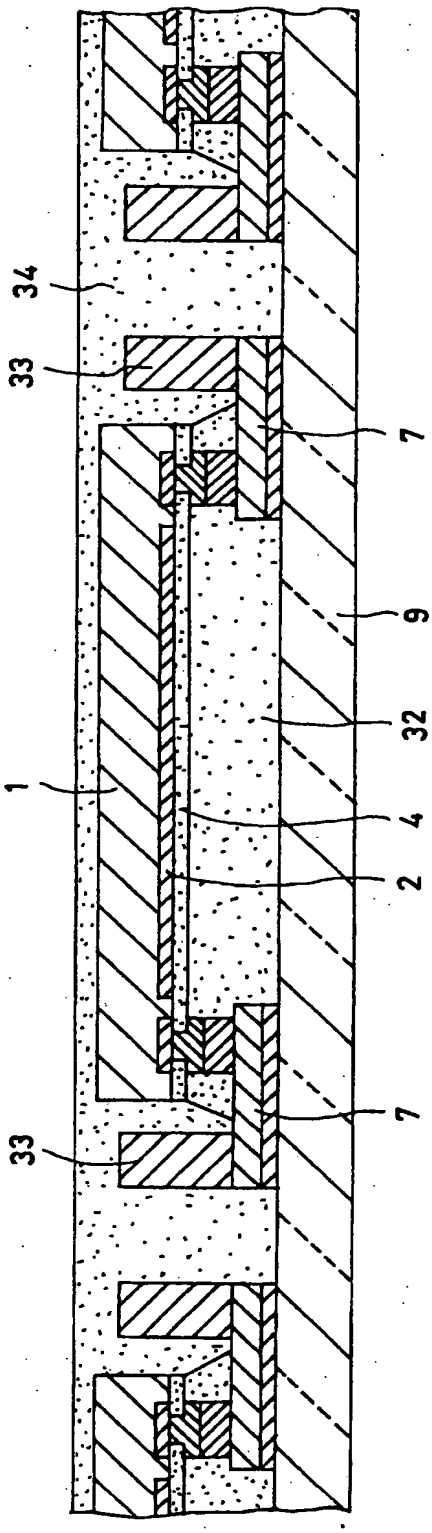
7
31
9
32
4
2
30
3
31
7
33

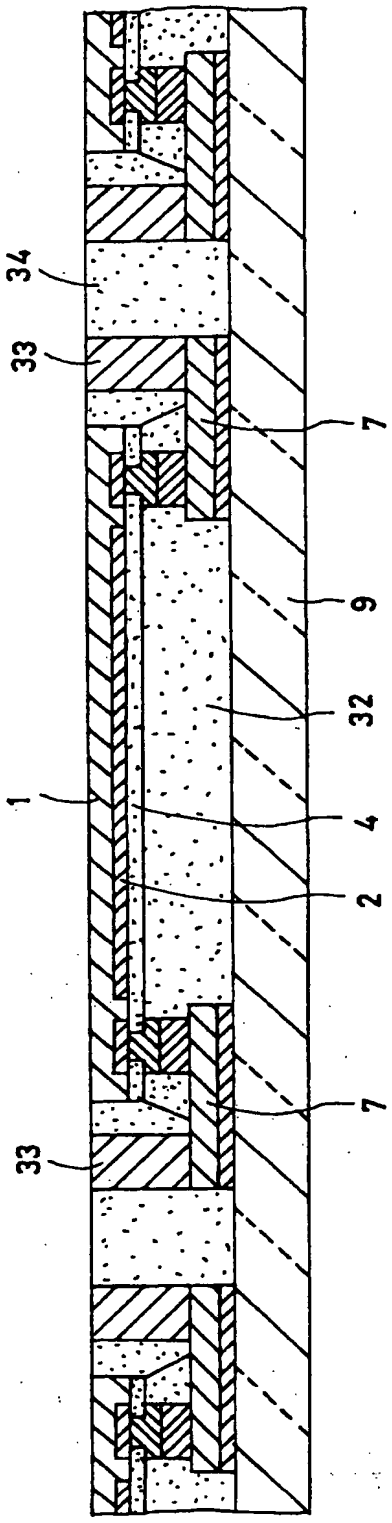
【図１９】

FIG. 19



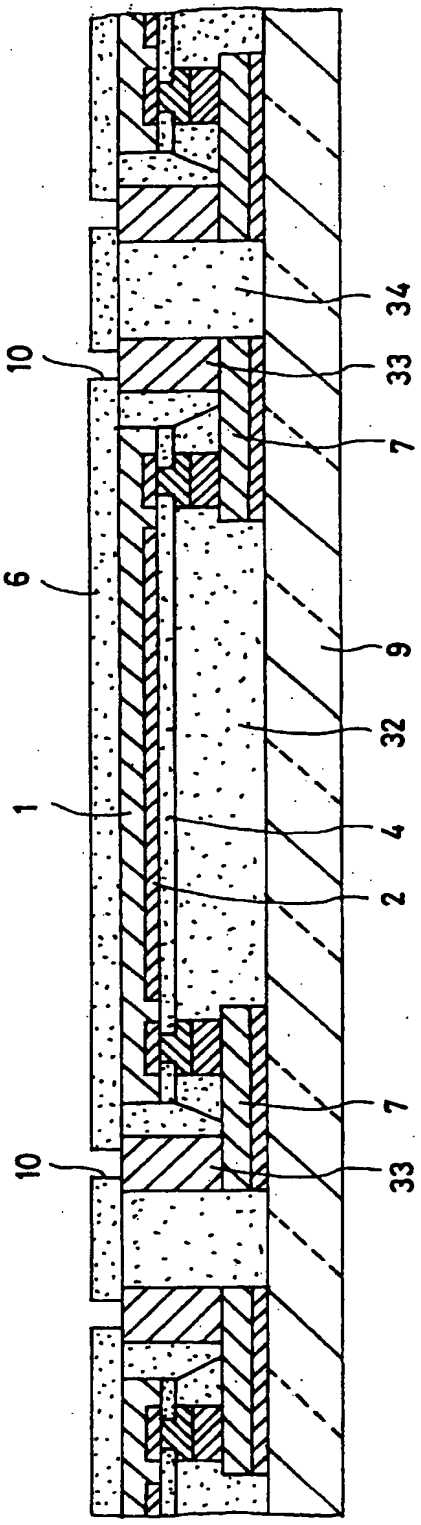
【図２０】

FIG. 20



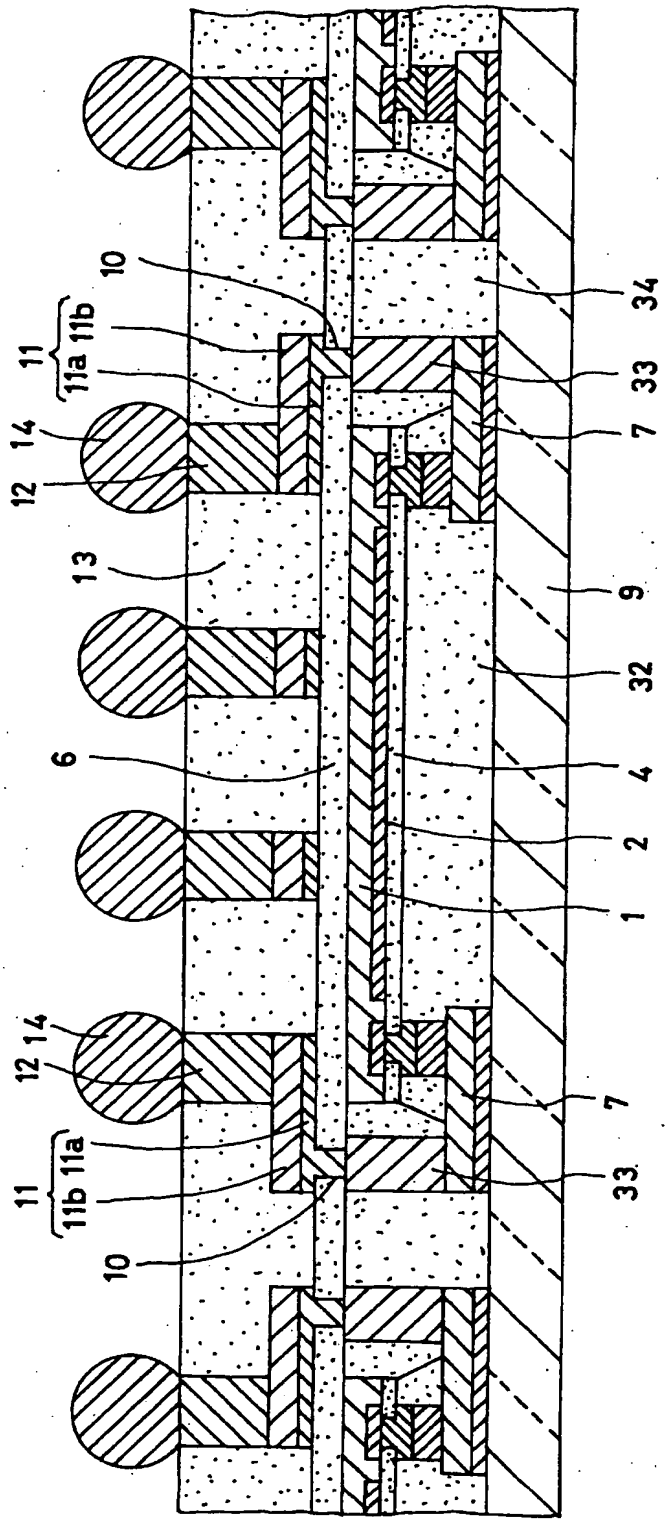
【図２１】

FIG. 21



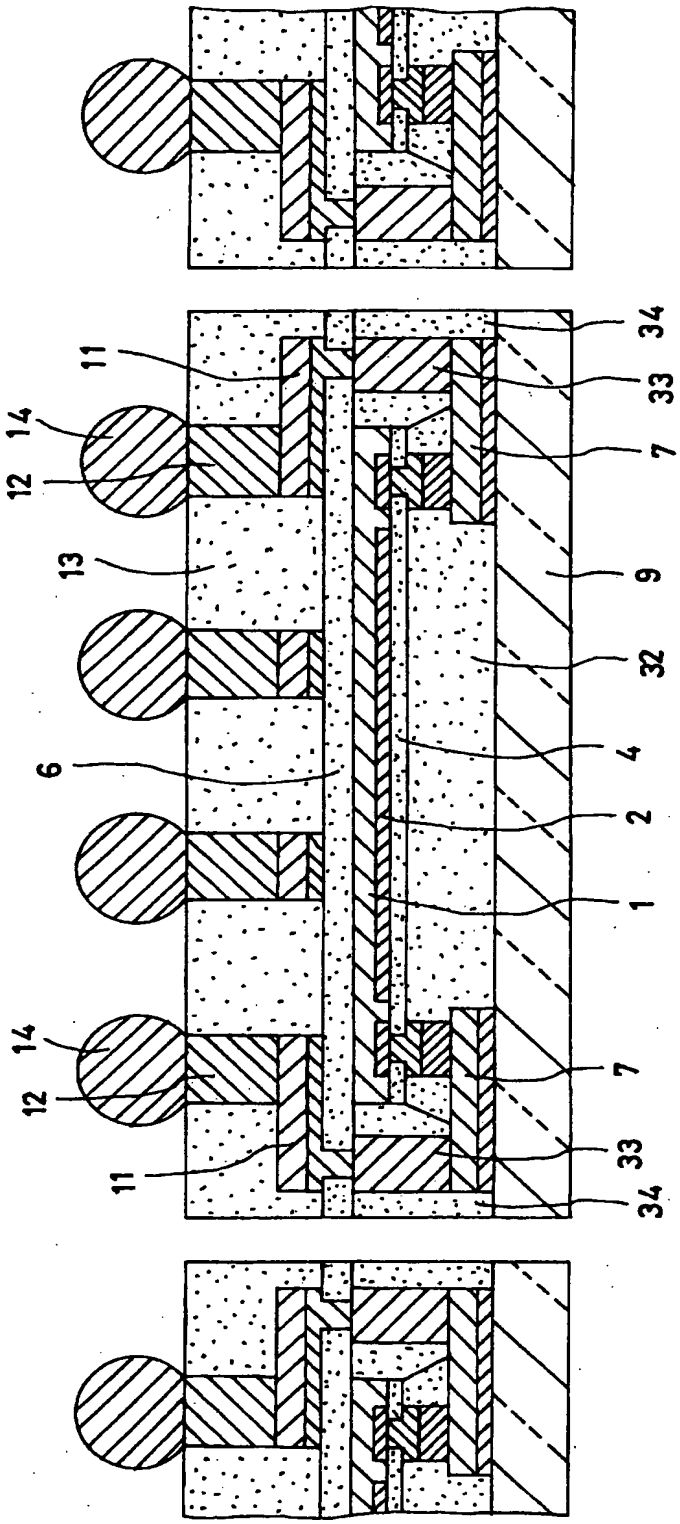
【図２２】

FIG. 22



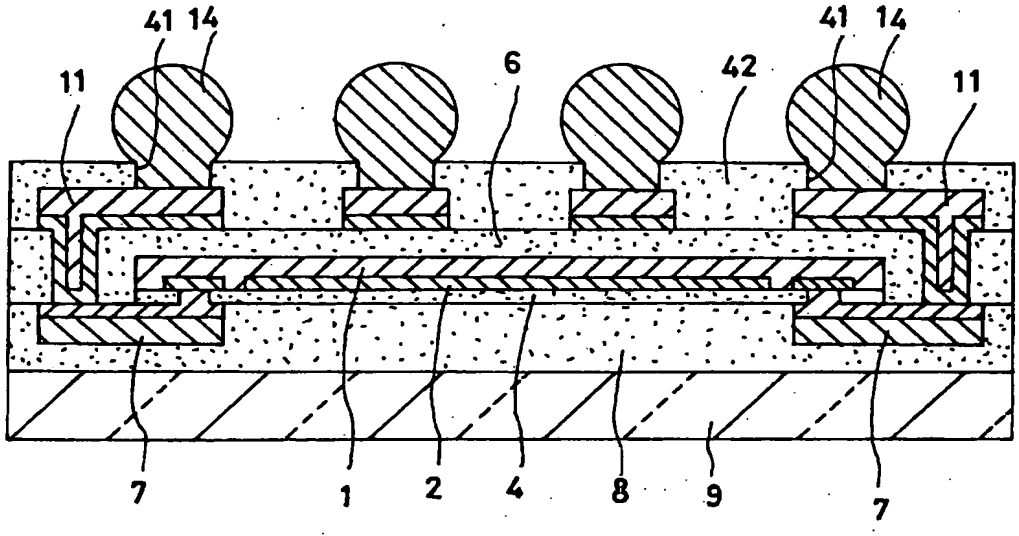
【図２３】

FIG. 23



【図２４】

FIG. 24



[Document] ABSTRACT

[Abstract]

[Object] To decrease a thickness of a semiconductor package provided with a photoelectric conversion device region such as a CCD, and increase its productivity.

[Means for Achieving the Object(s)] Silicon substrates 1 each having a photoelectric conversion device region 2 on its lower surface are attached to a transparent adhesive layer 8 on a glass substrate 9 having a size corresponding to a plurality of semiconductor packages/ In this case. A connecting wire 7 is provided to be connected to a connecting pad 3 of the silicon substrate 1, around the lower surface of the silicon substrate 1. An insulating film 6, distribution wire 11, columnar electrode 12, encapsulating film 13, and solder ball 14 are formed, the assembly is cut between the silicon substrates 1 to obtain a plurality of semiconductor packages each having a photoelectric conversion device region.

[Elected Figure] FIG. 14

Recognized Data · Added Data

Patent Application No.	Patent Application No. 2002-274807
Reception No.	No. 50201411235
Name of Document	PATENT APPLICATION
Official in Charge	Senior Official of the 5th Group 0094
Date of Preparation	September 24, 2002

<Recognized Data · Added Data>

[Filing Date] September 20, 2002

APPLICANT'S PAST DATA

Identification Number [000001443]

1. Date of Change August 10, 1990

[Reason for Change] New Registration

Address: 6-1, Nishishinjyuku 2-chome,
Shinjyuku-ku, Tokyo

Name: CASIO COMPUTER CO., LTD

2. Date of Change January 9, 1998

[Reason for Change] Change of Address

Address: 6-2, Hon-machi 1-chome,
Shibuya-ku, Tokyo

Name: CASIO COMPUTER CO., LTD